

Fig. 1

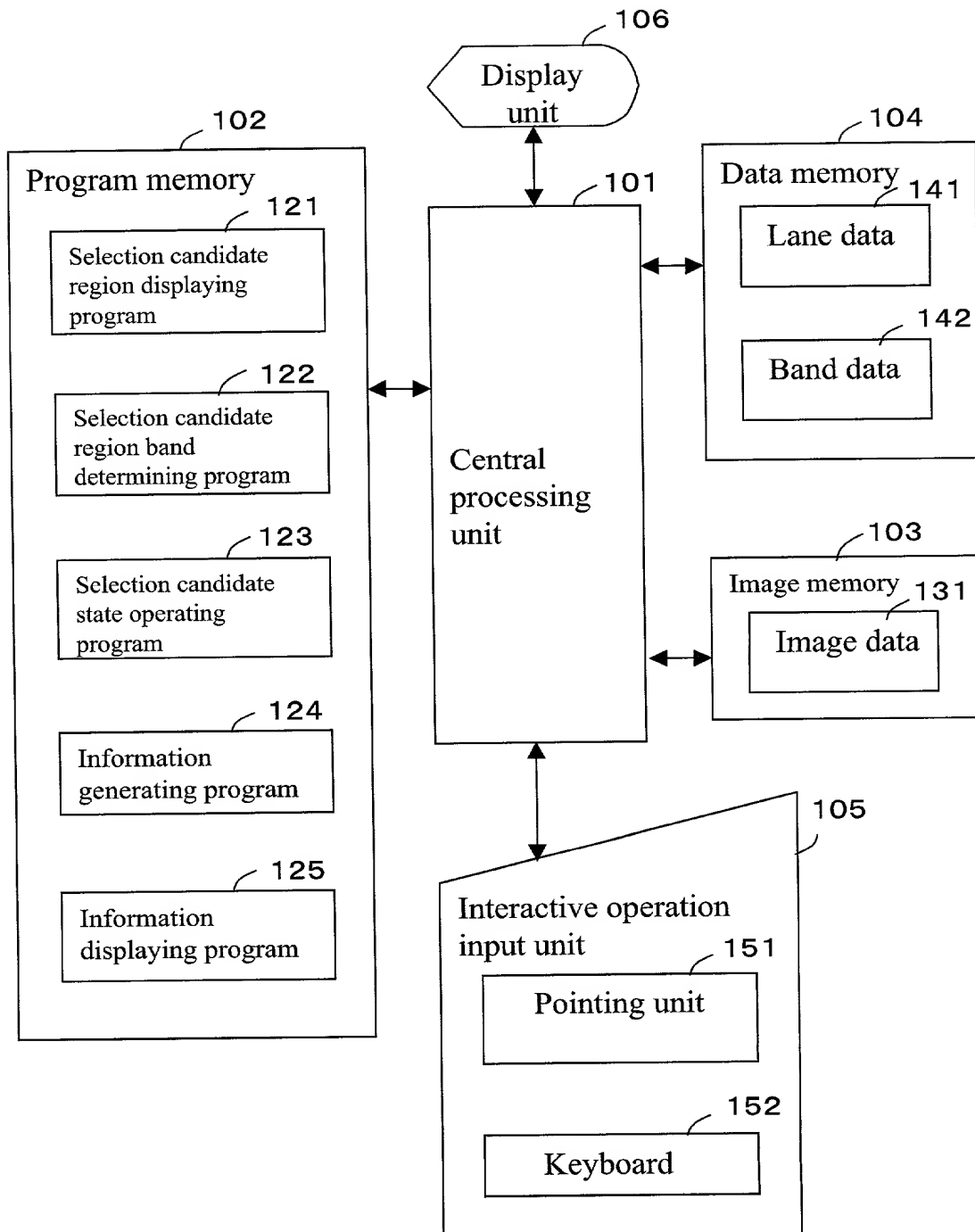


Fig. 2

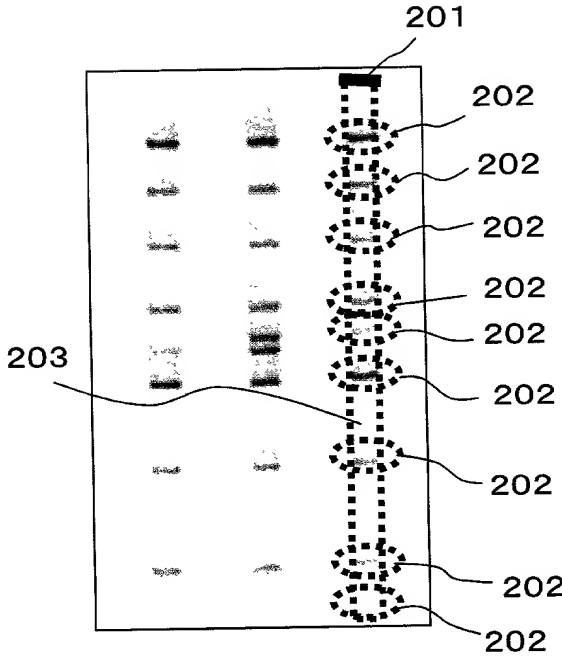


Fig. 3

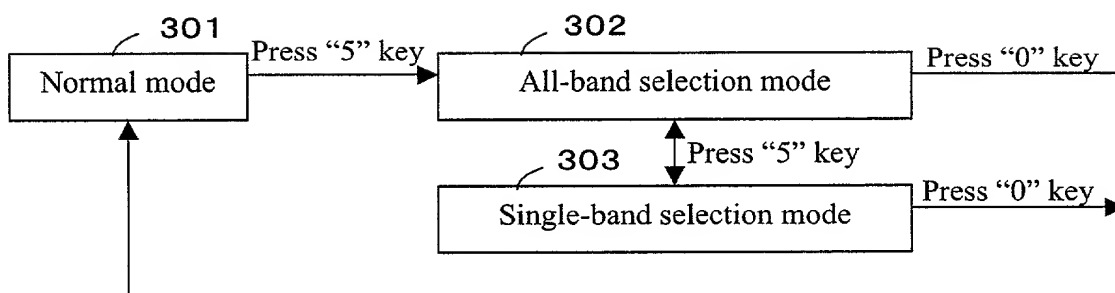


Fig. 4

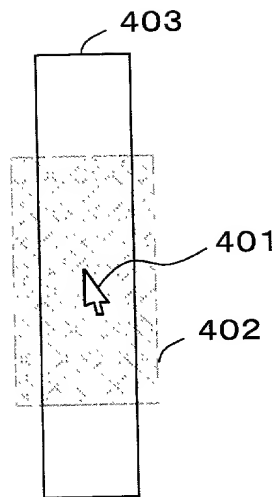


Fig. 5

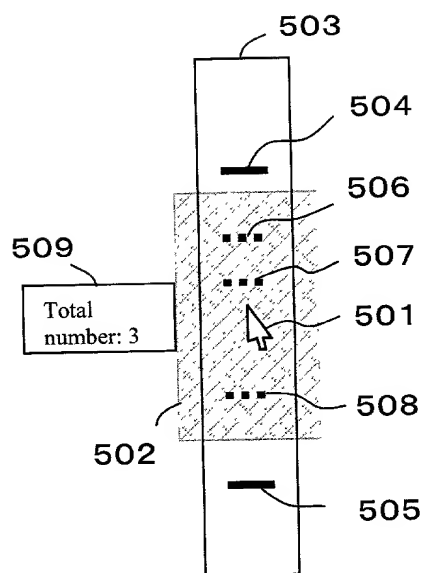


Fig. 6

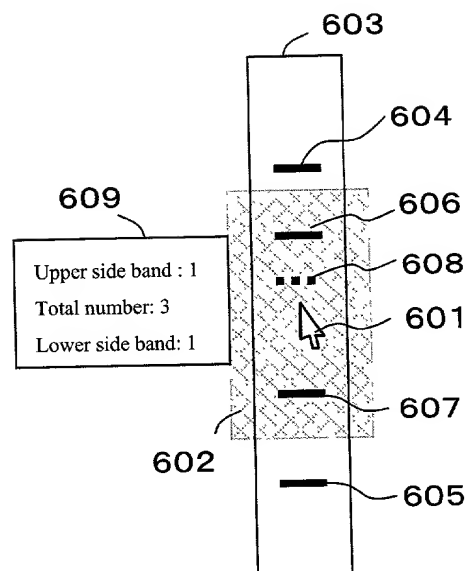


Fig. 7

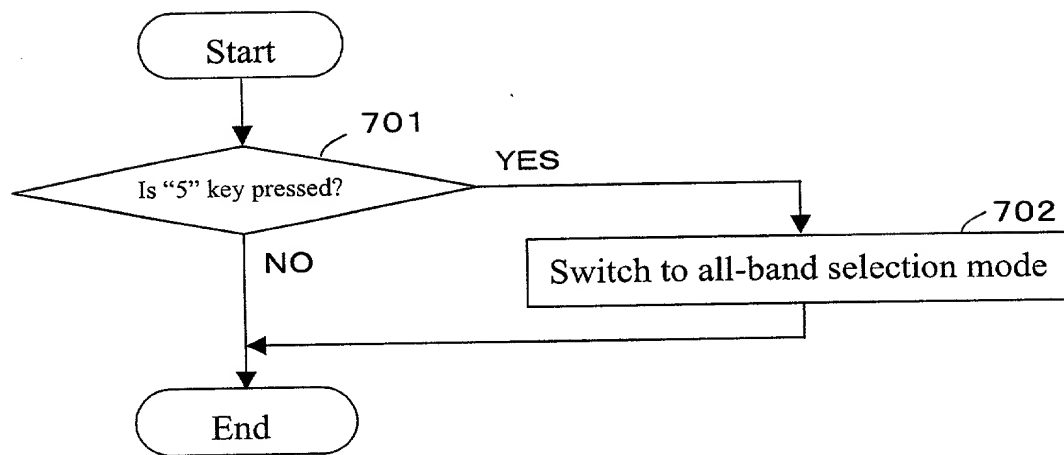


Fig. 8

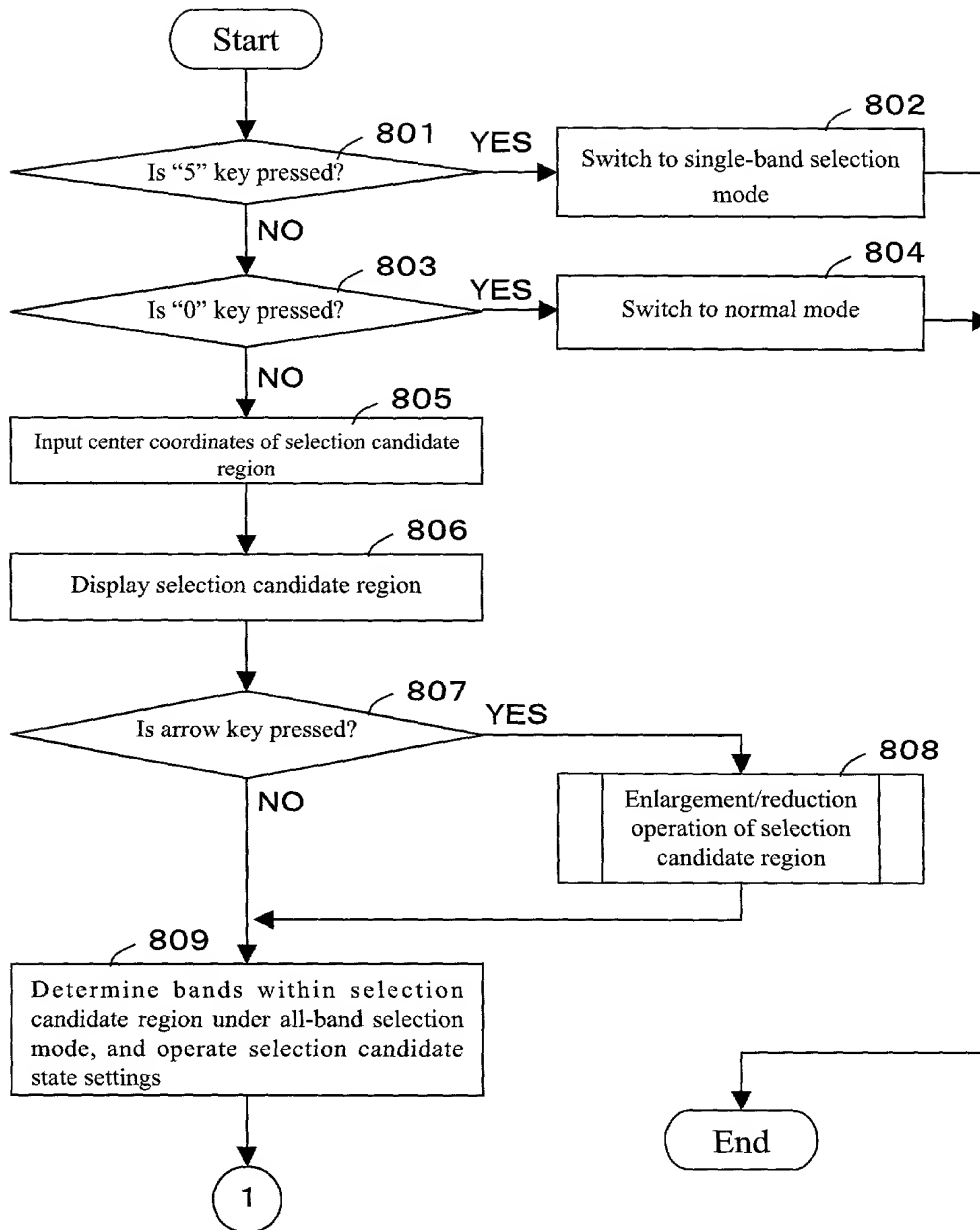


Fig. 9

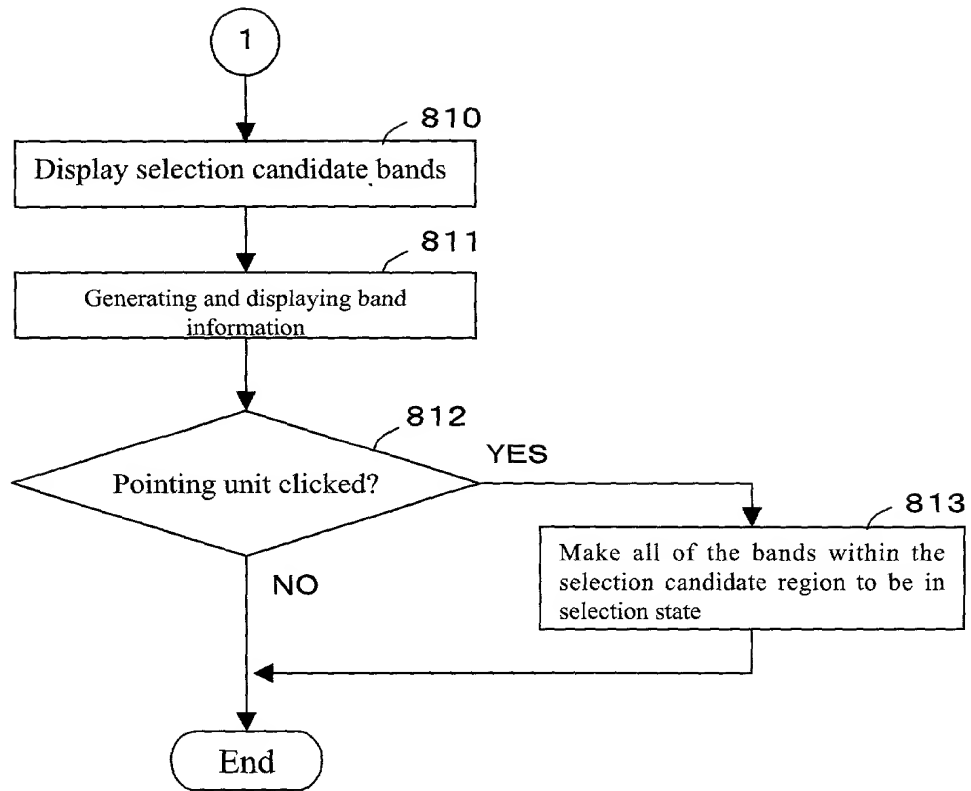


Fig. 10

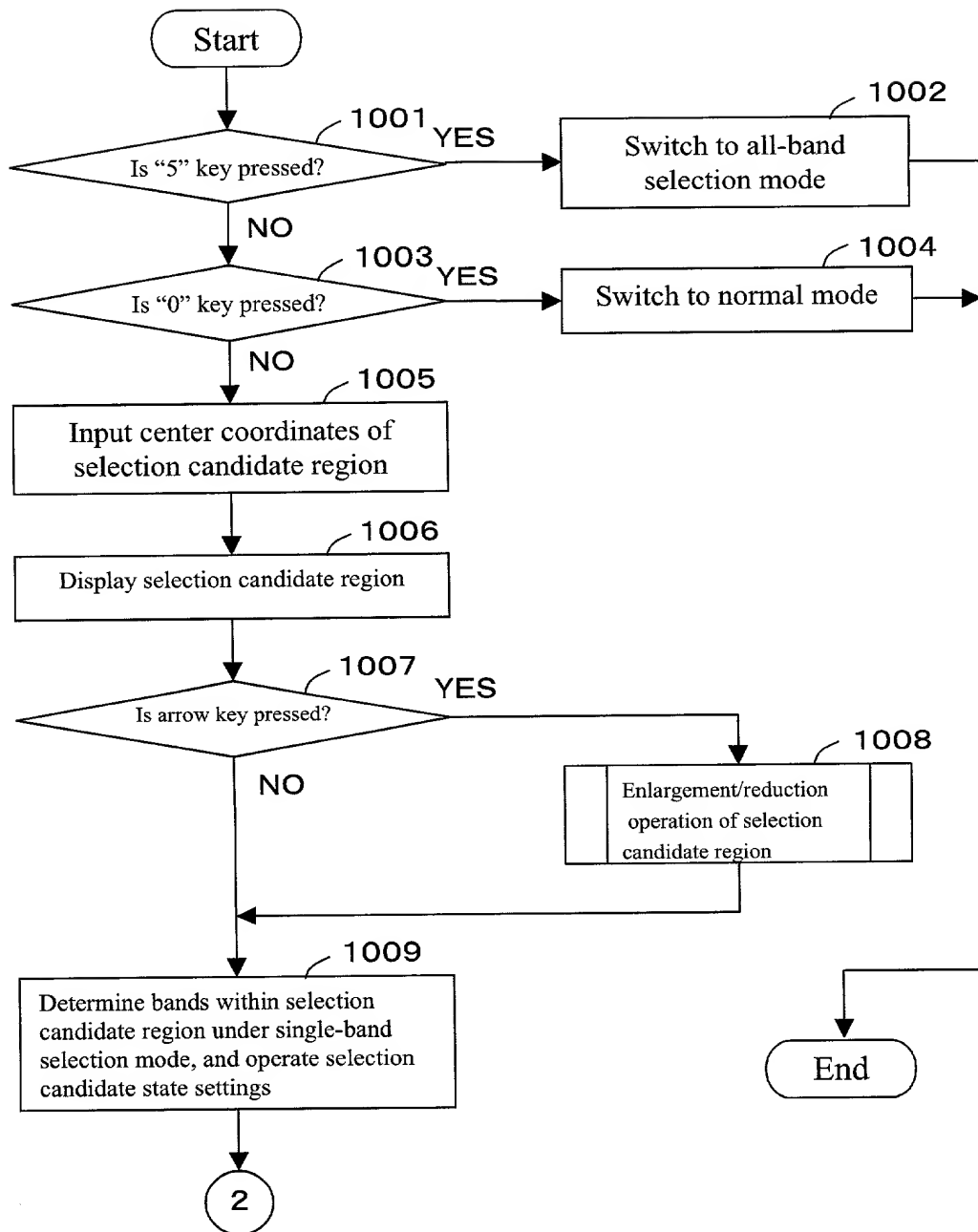


Fig. 11

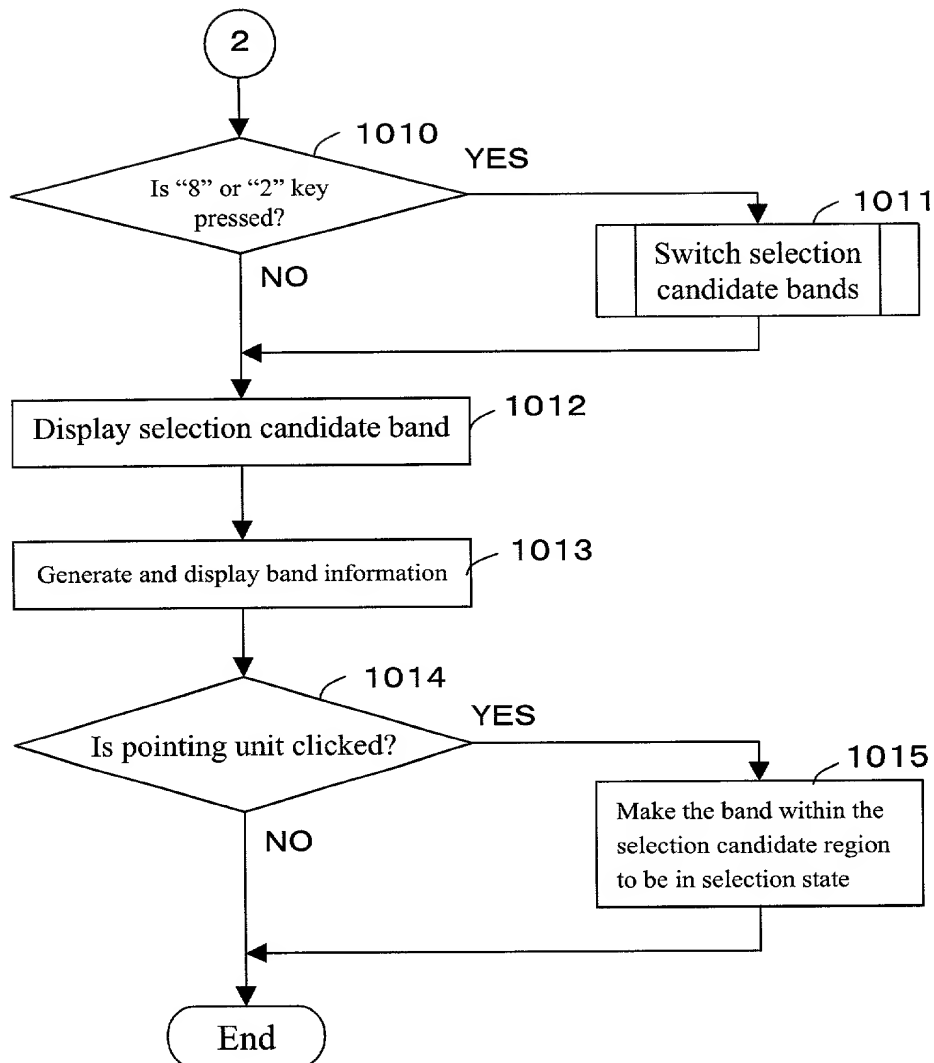
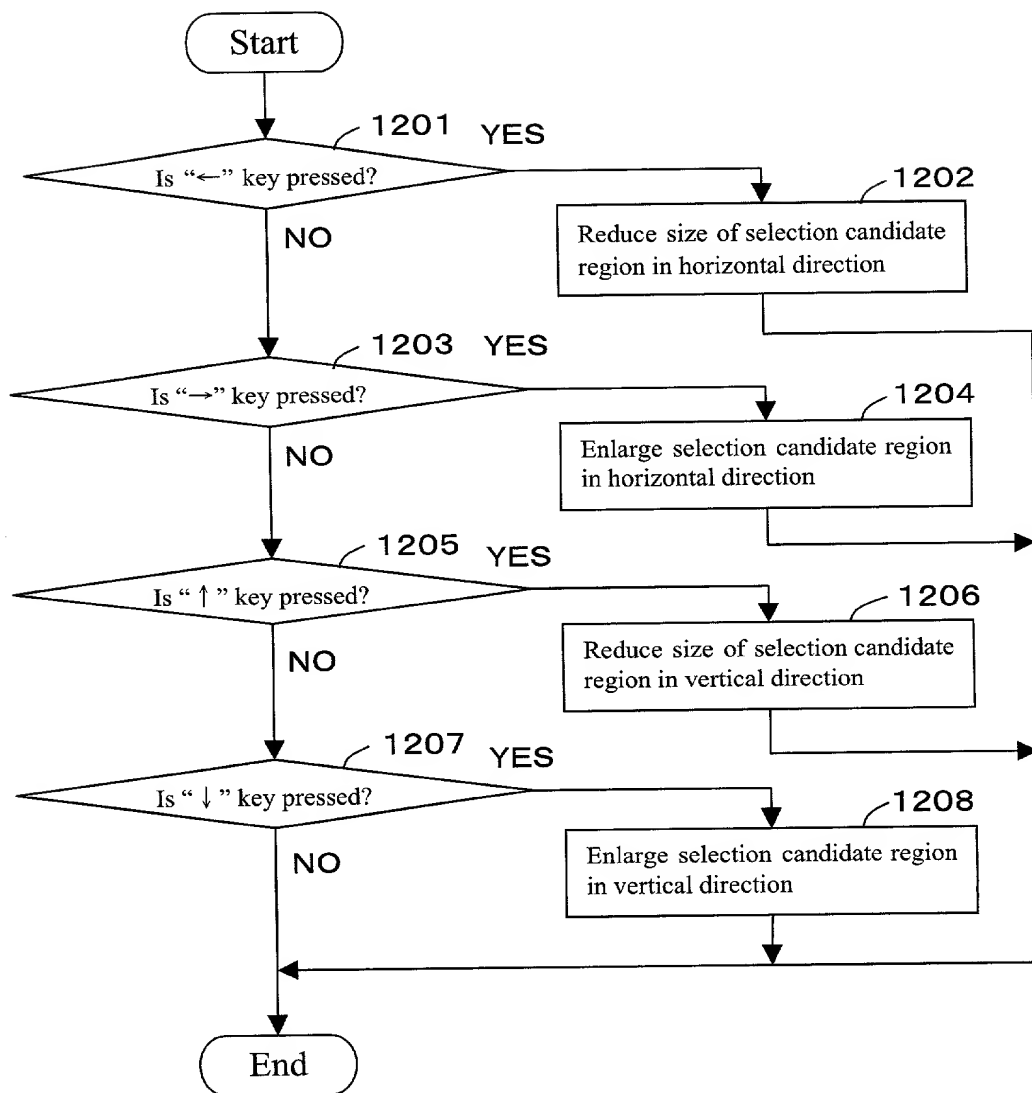


Fig. 12



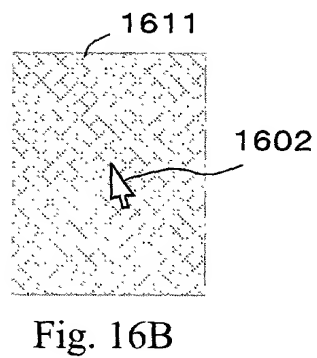
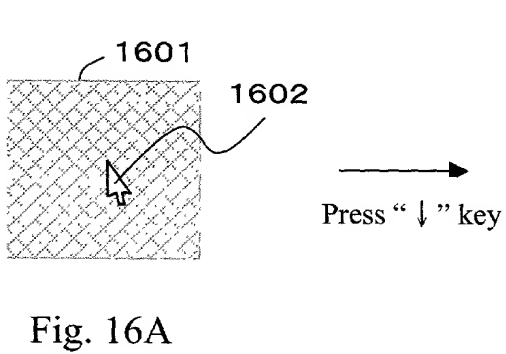
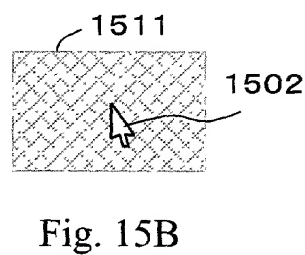
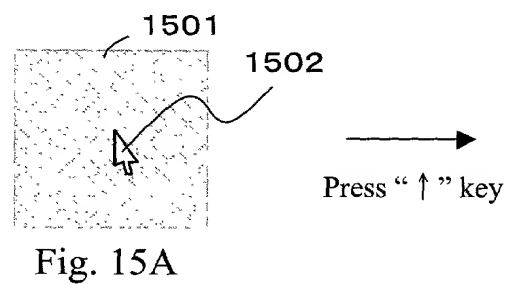
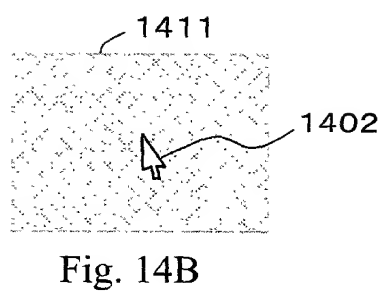
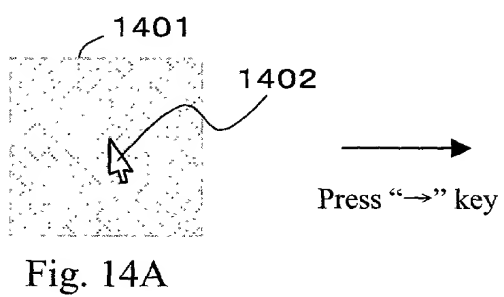
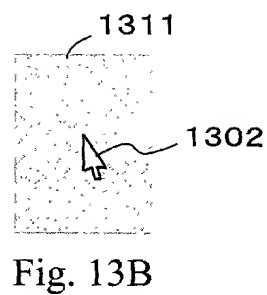
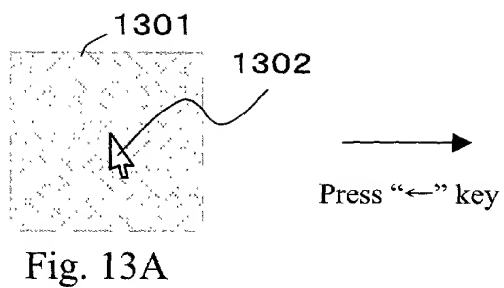


Fig. 17

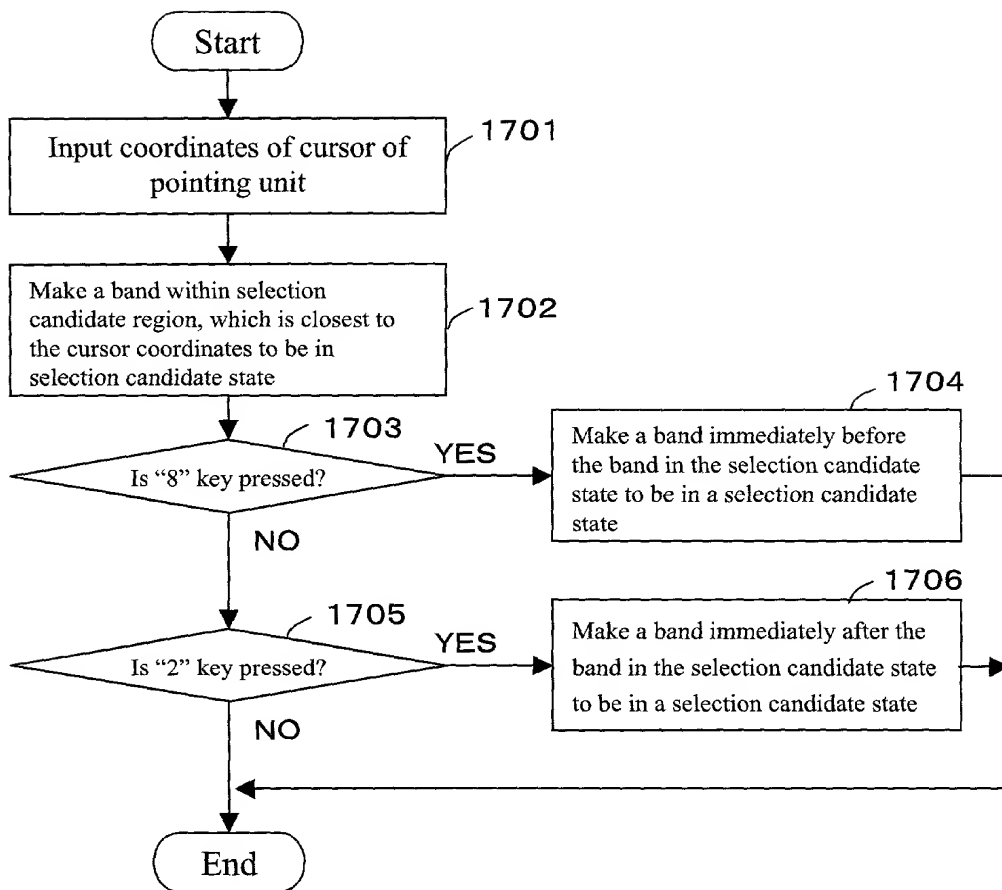


Fig. 18

Structure of data memory

Number of lanes	N	
Lane 1 data	Center coordinates (Y1U, X1S) of the upper end of Lane 1	
	Width (W1S) of upper end of Lane 1	
	Center coordinates (Y1E, X1E) of the lower end of Lane 1	
	Width (W1E) of the lower end of Lane 1	
	Number of bands (M1) in Lane 1	
	Band data of Lane 1	Relative coordinates (D1-1) of Band 1 with respect to the upper end of Lane 1
		Relative coordinates (D1-2) of Band 2 with respect to the upper end of Lane 1
		:
Relative coordinates (D1-M1) of Band M1 with respect to the upper end of Lane 1		
Lane 2 data		
:		
Lane N data		

Fig. 19

